AN APPROACH TO AUTOMATIC CIRCUIT DESIGN USING GENERAL-PURPOSE CIRCUIT SIMULATORS

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In this work an approach to automated design of the analog circuits is developed using the standard circuit simulator OrCAD PSpice. The realization of this approach is based on the principles of analog behavioral modeling. The input data, the design conditions and limitations are described using the possibilities of the Spice input language, which allows the inclusion of the complex functional dependencies between the design quantities. The different design stages are presented using the corresponding modules: calculation of the nonlinear distortion coefficient and the standard value determination of a capacitor. These modules are realized by autonomous computer modules and can be used in different design procedures.

Keywords: *OrCAD PSpice*, automated design, analog circuit

1. INTRODUCTION

The major problem in electronic design automation is the lack of flexible strategies and systematic techniques, which are required for a computer aided approach to the description and design of analog circuits.

Large-scale analog electronic circuits are often constructed from the few well-known basic building blocks, e.g. common-emitter stages, or differential pairs. Although the topology of such a building block is fixed, its elements values may vary strongly depending on the application. Calculating the correct element sizes for given circuit structures and specifications is one of the key tasks in analog circuit design [1].

The analog electronic design can be realized using specialized programs for circuit design, as well as using the possibilities of the standard circuit simulators. The second approach has several advantages. The design procedures are realized by solving linear and nonlinear algebraic systems of equations. In this case the suitable realization of the design procedures is the DC analysis of the standard circuit simulator.

2. MODULE FOR THE CALCULATION OF NONLINEAR DISTORTION COEFFICIENT

The nonlinear distortion coefficient is needed for the realization of the design procedure of the power amplifier, controlled by an operational amplifier [2,3]. A procedure for an automated determination of this coefficient is developed consisting of the following steps:

The current $I_{C\max 1}$ is defined using the dependence $I_{C\max 1} \geq I_{Lm}$. The base current $I_{B\max}$ is determined on the base on the calculated value of the current $I_{C\max 1}$ of the

used transistors from the output characteristic. The collector current ic' corresponds to the value of the base current $I_{B\max}/2$.

The coefficient of an asymmetry *b* has a value in the range $(b = 0.05 \div 0.4)$.

2.1 Introducing of the input data

The input data for this step are load current I_{Lm}, initial collector current I_C, supply voltage U_{CC}, coefficient of asymmetry *b,* load R_L.

The input data are introduced using the option *.PARAM* [4]:

.param ILm=7.785e-1,IC=7.785e-3,b=0.2,UCC=6.014V,RL=5

*.param ICmax1={1.2*ILm}*

2.2 Determination of $I_{B\max}$

The nulor model is presented using the controlled source by the gain coefficient of value 10^{10}. The nulor model is used to determinate the current $I_{B\max}$. The equivalent circuit is presented in Fig.1.

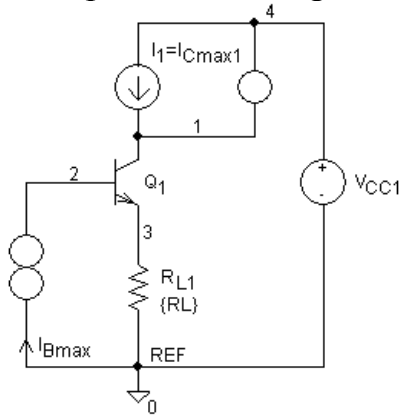

Fig.1. Determination of the current I_{Bmax}

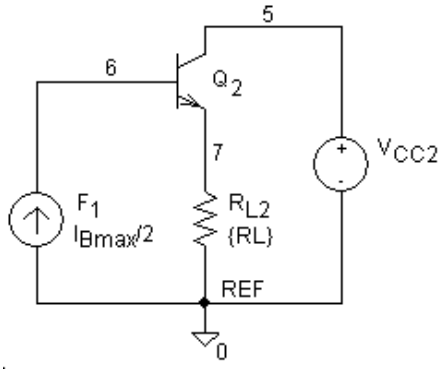

Fig.2. Equivalent circuit for the determination of the collector current *ic'*

The voltage V(1,4) is set at zero value by introducing the nullator between nodes 1 and 4. The norator ensures a current path for the base current $I_{B\max}$ of the transistor, corresponding with the defined collector value $I_{C\max 1}$. The independent voltage source *VPROB* type is used as a short-circuit branch.

ENOR DOP REF 1 4 1E10

VPROB 2 DOP DC 0

The collector current $I_{C\max 1}$ and the supply voltage U_{CC} are applied using the independent current and voltage source of *I* and *V* type.

I1 4 1 DC {ICmax1}

VCC1 4 REF DC {UCC}

2.3 Determination of ic'

The collector current ic' is determined using the equivalent circuit, shown in Fig.2.

The base current of the transistor Q_2 is equal to the current $I(V_{PROB})$ with the coefficient 0.5. The *PSpice* presentation is realized using the current controlled current source *F*1.

F1 5 REF VPROB 0.5

The current controlled current source *F*2 is used to obtaining the collector current ic', correspond to $I_{B\max}/2$:

F2 REF Ic1 VCC2 –1
RF2 REF Ic1 1

2.4 Calculation of the harmonic amplitudes

The determination of the harmonic amplitudes is realized using the following equations [2,3]:

$$I_{\max} = (1+b) * I_{C\max 1}, I_{\min} = (-(1-b)) * I_{C\max 1} \quad (1)$$

$$i' = (1+b) * ic' \ , i'' = -(1-b) * ic' \quad (2)$$

$$I' = 2 * b * I_C \quad (3)$$

$$I_{1m} = \frac{1}{3}\left(I_{\max} - I_{\min} + i' + i''\right) = \frac{2}{3}\left[I_{C\max 1} - ic'\right] \quad (4)$$

$$I_{2m} = \frac{1}{4}\left(I_{\max} + I_{\min} - 2 * I'\right) = \frac{b}{2}\left[I_{C\max 1} - 2 * I_C\right] \quad (5)$$

$$I_{3m} = \frac{1}{6}\left[I_{\max} - I_{\min} - 2 * \left(i' - i''\right)\right] = \frac{1}{3}\left[I_{C\max 1} - 2 * ic'\right] \quad (6)$$

$$I_{4m} = \frac{1}{12}\left[I_{\max} + I_{\min} - 4 * \left(i' + i''\right) + 6 * I'\right] = \frac{b}{6}\left[I_{C\max 1} - 4 * ic' + 6 * I_C\right] \quad (7)$$

The harmonic amplitudes I_{1m}, I_{2m}, I_{3m} и I_{4m} are described using the GVALUE elements of *ABM* library, according to the input language of *OrCAD Pspice* and the equations (4), (5), (6), (7).

GI1H REF I1H VALUE={0.6667(ICmax1-V(Ic1))}*
RI1H REF I1H 1
*GI2H REF I2H VALUE={0.5*b*(ICmax1-(2*IC))}*
RI2H REF I2H 1
*GI3H REF I3H VALUE={(ICmax1-(2*V(Ic1)))/3}*
RI3H REF I3H 1
*GI4H REF I4H VALUE={(ICmax1-(4*V(Ic1))+(6*IC))*(b/6)}*
RI4H REF I4H 1

2.5 Determination of the nonlinear distortion coefficient K_h

The nonlinear distortion coefficient is determined by the equation [2,3]:

$$K_h = \frac{\sqrt{I_{2m}^2 + I_{3m}^2 + I_{4m}^2}}{I_{1m}^2} \quad (8)$$

The calculation of the nonlinear distortion coefficient K_h is represented using the *GVALUE* element.

```
GKh REF Kh VALUE={SQRT(V(I2H)*V(I2H)+V(I3H)*V(I3H)+
+V(I4H)*V(I4H))/(V(I1H) *V(I1H)+1e-10)}
RKh REF Kh 1
```

```
.lib nom.lib
.model TR_npn NPN
+ (Is=2.447p  Xti=3  Eg=1.11  Vaf=100  Bf=208.2
.....................................................................
Xtf=5.945 Vtf=10 Rb=.1)

.param ILm=7.785e-1,IC=7.785e-3
.param b=0.2,UCC=6.014V
.param RL=5,Kx=0.01,ICmax1={1.2*ILm}
VGND REF 0 0

Q1 1 2 3  TR_npn
I1 4 1 DC {ICmax1}
VPROB 2 DOP DC 0
ENOR DOP REF 1 4 1E10
VCC1 4 REF DC {UCC}
RL1 3 REF {RL}

Q2 5 6 7 TR_npn
F1 6 REF VPROB 0.5
VCC2 5 REF DC {UCC}
RL2 7 REF {RL}

F2 REF Ic1 VCC2 -1
RF2 REF Ic1 1
```

```
GI1H REF I1H VALUE=+
+{0.6667*(ICmax1-V(Ic1))}
RI1H REF I1H 1
GI2H REF I2H VALUE=+
+{0.5*b*(ICmax1-(2*Ic))}
RI2H REF I2H 1
GI3H REF I3H VALUE=+
+{(ICmax1-(2*V(Ic1)))/3}
RI3H REF I3H 1
GI4H REF I4H VALUE=+
+{(ICmax1-(4*V(Ic1))+(6*IC))*(b/6)}
RI4H REF I4H 1

GKh REF Kh VALUE=+
+{SQRT(V(I2H)*V(I2H)+V(I3H)*V(I3H)+
+V(I4H)*V(I4H))/(V(I1H)*V(I1H)+1e-10)}
RKh REF Kh 1

.print dc V([Kh])
VICmax1 ICmax1 REF DC {ICmax1}
RICmax1 ICmax1 REF 1G
.print DC V([ICmax1])
.end
```

Fig.3. *PSpice* realization of the module for the calculation of nonlinear distortion coeffcient

```
NODE   VOLTAGE
(Kh) 3.10424040  (I1H) .21421107
(I2H) .09186300   (I3H)-.09719964  (I4H)-.04902293  (Ic1) .61289946  (ICmax1) .93420000
```

Fig.4. Simulation results

The *PSpice* realization of the module for the calculation of nonlinear distortion coeffcient is shown in Fig.3 and the simulation results are presented in Fig.4.

3. STANDARD VALUE DETERMINATION OF THE CAPACITOR

The standard value determination of the circuit element is an important part of the electronic circuit design. The selection of the standard value depends on the user-defined tolerance. The module for automated standard value determination is realized in correspondence to the input language of *OrCAD PSpice.*

3.1 Introducing of the input data

The calculated value of the investigated capacitor C_{cal} and the user-defined tolerance ε are introduced as input data using the option *.PARAM* [4]. The calculated

value of the capacitor must be presented in the normalized form: $X.10^N$, where X is the mantissa in the range $(1 \div 10)$ and N is the exponent.

.param Ccal=2.75p,EPS=20

3.2 Calculation of the exponent

The parameters C_{CAL_i} i=12,9,6 are used to calculate the exponent in accordance with the following equation:

$$C_{CAL\_i} = C_{CAL}.10^i \tag{9}$$

*.param Ccal12={Ccal*1e12}*

The value of the parameter C_{CAL_12} is compared with the value –12. In this case the parameter P_1 (participating in the exponent forming) obtains zero value and -12 otherwise.

The comparison is realized using the operator *IF*. It has a following form:

.param P1={if(Ccal12>=1,-12,0)}

Similarly, comparisons are made for the range nF und μF using parameter values *Ccal9* and *Ccal6*. The exponent P_3 is calculated by the expression:

.param P2={if(Ccal9>=1,3,0)}, P3={P1+P2+if(Ccal6>=1,3,0}

3.3 Determination of the mantissa

The mantissa value is in the range $(1 \div 1000)$ is calculated in the form:

$$C_{CAL\_m} = C_{CAL}.10^{|P_3|}. \tag{10}$$

The *PSpice* presentation of the Eq.(10) is:

*.param Ccalm={Ccal*pwr(10,abs(P3))}.*

In similar way the normalized mantissa in the range $(1 \div 10)$ is calculated using two additional divisions.

3.4 Introducing the standard capacitor values from the data base

The standard values corresponding to $\pm 5\%, \pm 10\%, \pm 20\%$ tolerance deviations are implemented in the program module. The standard value determination, corresponding to the $\pm 20\%$ derivation, is realized using .FUNC function, as shown in Fig.5.

```
.FUNC F20(X)={IF(X<=1.1,1.0,0)+
              +IF((X>1.1)&(X<=1.85),1.5,0)+
              +IF((X>1.85)&(X<=2.75),2.2,0)+
              +IF((X>2.75)&(X<=4.00),3.3,0)+
              +IF((X>4.0)&(X<=5.75),4.7,0)+
              +IF((X>5.75),6.8,0)}
```

Fig.5. Description of the standard capacitor values for the 20 %tolerance

3.5 Determination of the standard value of capacitor

The standard capacitor value C_{ST} is calculated using the following equation:

$$C_{ST} = F_{20}(C_{END}).10^{P_5}.L_{20} + F_{10}(C_{END}).10^{P_5}.L_{10} + F_5(C_{END}).10^{P_5}.L_5 \tag{11}$$

where Li={if((EPS=i),1,0)} i=5,10,20; EPS is the user-defined tolerance.

The *PSpice* realization of the Eq. (11) has a following form:

```
.param CST={F20(A7)*PWR(10,P5)*L20+
      +F10(A7)*PWR(10,P5)*L10+
      +F5(A7)*PWR(10,P5)*L5}
```

```
.param Ccal=2.75p,EPS=20

.param Ccal12={Ccal*1e12}
.param P1={if(Ccal12>=1,-12,0)}
.param Ccal9={Ccal*1e9}
.param P2={if(Ccal9>=1,3,0)}
.param Ccal6={Ccal*1e6}
.param P3={P1+P2+if(Ccal6>=1,3,0)}
.param Ccalm={Ccal*PWR(10,abs(P3))}
.param A5={Ccalm/10}
.param P4={P3+if(A5>=1,1,0)}
.param A6={A5/10}
.param P5={P4+if(A6>=1,1,0)}
.param A7={Ccal*pwr(10,abs(P5))}
.FUNC F20(X)={IF(X<=1.1,1.0,0)+
      ……..
        +IF((X>5.75),6.8,0)}
.FUNC F10(X)={IF(X<=1.1,1.0,0)+
      ……..
        +IF((X>7.5),8.2,0)}
.FUNC F5(X)={IF(X<=1.05,1.0,0)+
      ……..
        +IF((X>8.65),9.1,0)}
.param B1={20-EPS},B2={10-EPS}+
+B3={5-EPS}
.param L20={if(B1==0,1,0)}+
      +L10={if(B2==0,1,0)}+
      +L5={if(B3==0,1,0)}
.param CST={F20(A7)*PWR(10,P5)*L20+
      +F10(A7)*PWR(10,P5)*L10+
      +F5(A7)*PWR(10,P5)*L5}
VCSTAND CSTAND 0 DC {CST}
RCSTAND CSTAND 0 1G
.print DC V([CSTAND])
.end
```

Fig.6. *PSpice* realization of the module for determining the standard value of the capacitor

```
NODE   VOLTAGE
(CSTAND) 2.200E-12
```

Fig.7. Calculating value of the capacitor

The *PSpice* realization of the module for the standard value determination of capacitor is shown in Fig.6 and the simulation results are presented in Fig.7.

4. CONCLUSION

In this paper an approach to automated circuit design have been developed using the possibilities of the standard circuit simulator *OrCAD PSpice*. The modules for a calculation of the nonlinear distortion coefficient and the standard value determination of a capacitor are presented. These modules can be used in another design amplifier procedures.

5. REFERENCES

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Our PEPS-based simulator is a general-purpose quantum circuit simulator for arbitrary quantum circuits: it stores the full quantum state and it can be readily used to compute single amplitudes, observables, and also per-form sequences of quantum measurements. While the quantum circuit simulator we present can tackle generic circuits, in the following we focus on RQCs.Â Quantum Circuit Simulator Based on PEPS. In the following we consider a two-dimensional rectangular lattice of size Lv Ã—Lh, where Lv and Lh are, respectively, the sizes in the vertical and horizontal directions.Â This simula-tor can be used to store eectively highly entangled wave-functions, and it is readily adaptable to compute expec-tation values or simulate sequential quantum measure-ments. This is an electronic circuit simulator. When the applet starts up you will see an animated schematic of a simple LRC circuit. The green color indicates positive voltage. The gray color indicates ground. A red color indicates negative voltage. The moving yellow dots indicate current. To turn a switch on or off, just click on it. If you move the mouse over any component of the circuit, you will see a short description of that component and its current state in the lower right corner of the window. To modify a component, move the mouse over it, click the right mouse button (or control-click if y General purpose circuit simulators are usually based on the nodal approach, solving the node voltages of a circuit. Here, the natural building blocks for the component models are controlled current and charge sources [6,7]. This approach results in an inverse analogy between mechanical and electrical quantities. The models in the circuit simulation tool APLAC [6,7] are based on the use of static and dynamic voltage-controlled current sources.Â An automatic optimization process is used for finding suitable values for the parasitic components and the intrinsic current sources. The intrinsic model is created with the use of frequency-dependent current sources. VHDL allows circuit synthesis as well as circuit simulation (both are covered in the book). The former is the translation of a source code into a hardware structure that imple-ments the intended functionality, while the latter is a testing procedure to ensure that such functionality is indeed achieved by the synthesized circuit. In all chapters we will concen-trate on VHDL constructs that are synthesizable, except for chapter 10, which deals exclu-sively with VHDL for simulation. Electronic circuit simulation uses mathematical models to replicate the behavior of an actual electronic device or circuit. Simulation software allows for modeling of circuit operation and is an invaluable analysis tool.Â Simulating a circuitâ€™s behavior before actually building it can greatly improve design efficiency by making faulty designs known as such, and providing insight into the behavior of electronics circuit designs. In particular, for integrated circuits, the tooling (photomasks) is expensive, breadboards are impractical, and probing the behavior of internal signals is extremely difficult. Therefore, almost all IC design relies heavily on simulation.Â The event driven algorithm provided by mixed-mode simulators is general purpose and supports non-digital types of data.